ABSTRACT

A reconfigurable memory in an integrated circuit includes an array of memory cells and a memory controller. The array of memory cells in the reconfigurable memory are tested to determine if they are unusable and if so, their associated physical addresses corresponding to their physical location. After determining the physical addresses where any failure exists, the physical addresses locations associated with the physical locations of unusable memory cells or memory blocks are mapped out to avoid addressing them. While mapping out unusable memory locations or memory blocks reduces the total capacity, the reconfigurable memory has sufficient capacity for the integrated circuit to remain functionally usable.